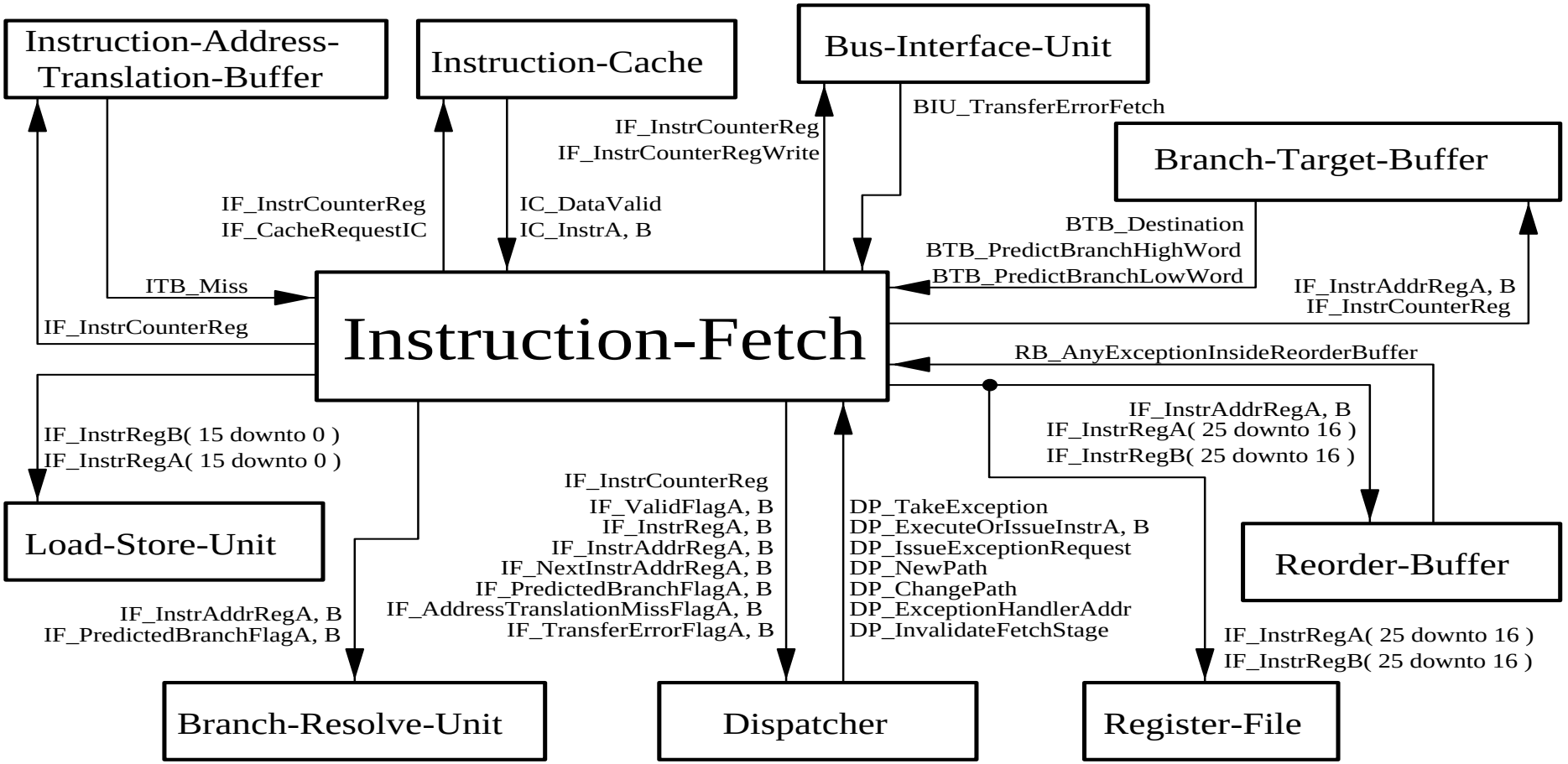
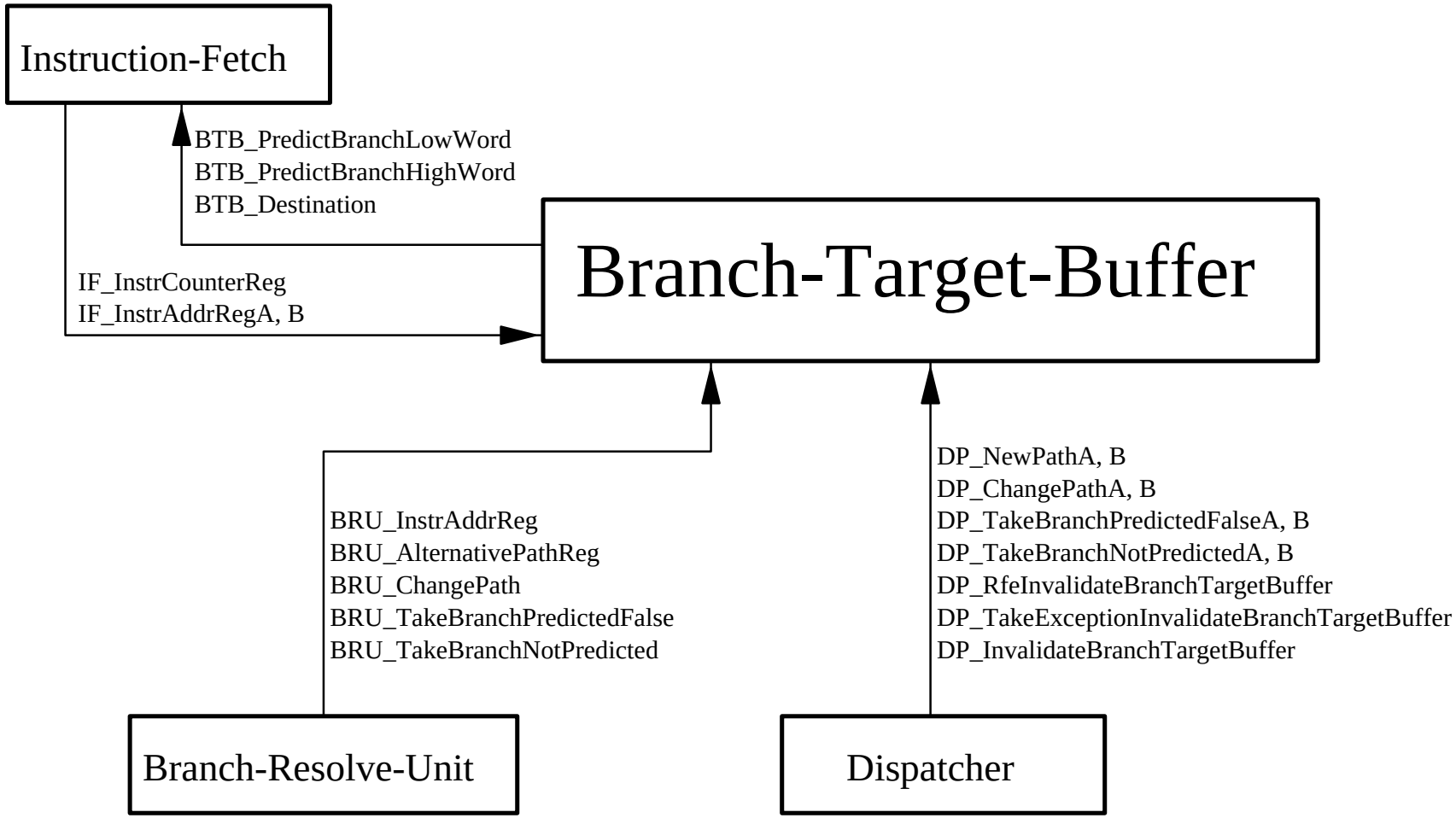
Interfaces aller Entwurfseinheiten

Die folgenden Abbildungen zeigen jeweils alle Eingangs- und Ausgangssignale einer Entwurfseinheit. Diese Übersicht ist nützlich, um das Zusammenwirken der einzelnen Module in der DLX zu erfassen.
Die Teilsysteme sind in der Reihenfolge abgedruckt, in der sie auch in der VHDL-Datei 'Dlx.vhd' zu finden sind.

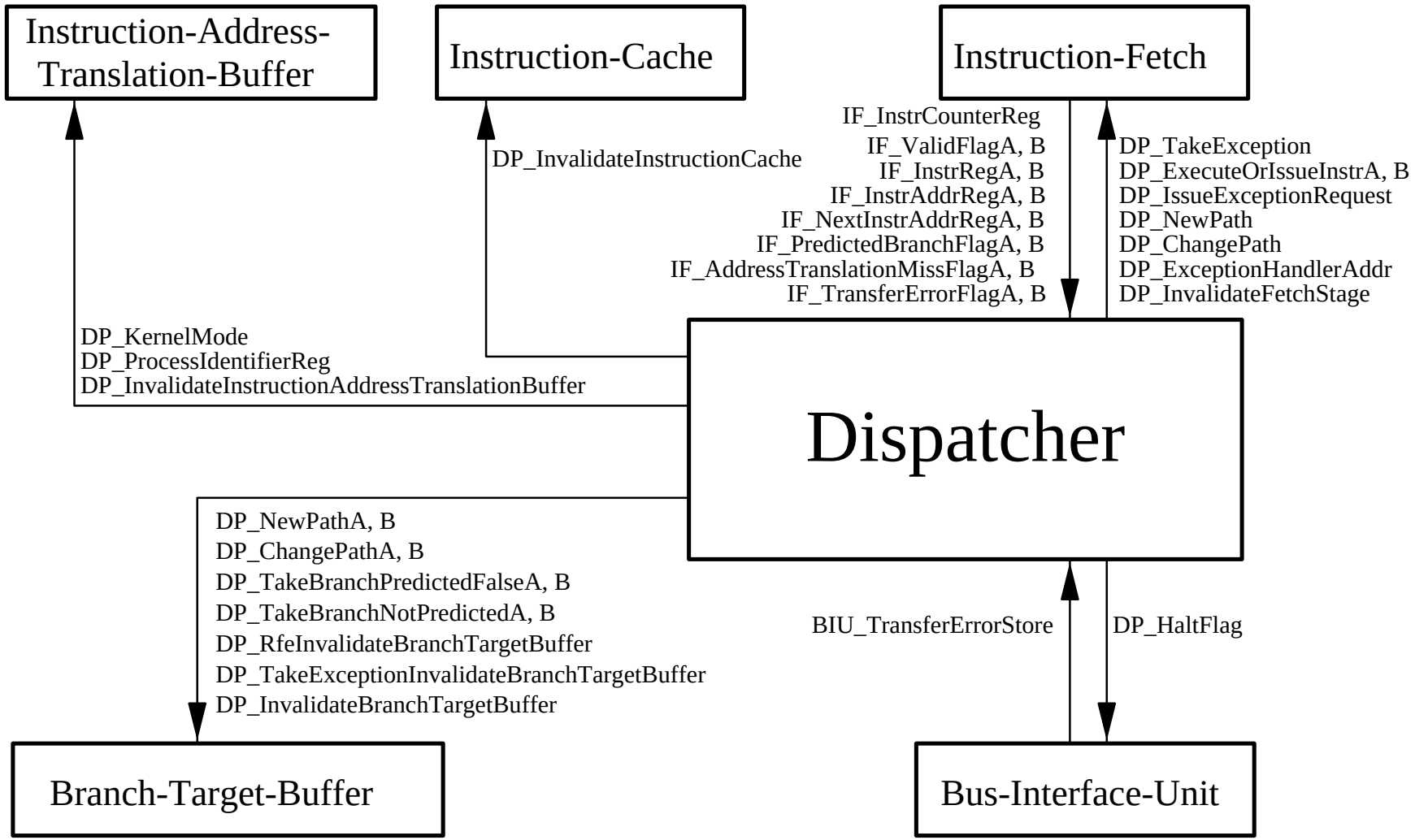
Interface of the Instruction-Fetch unit



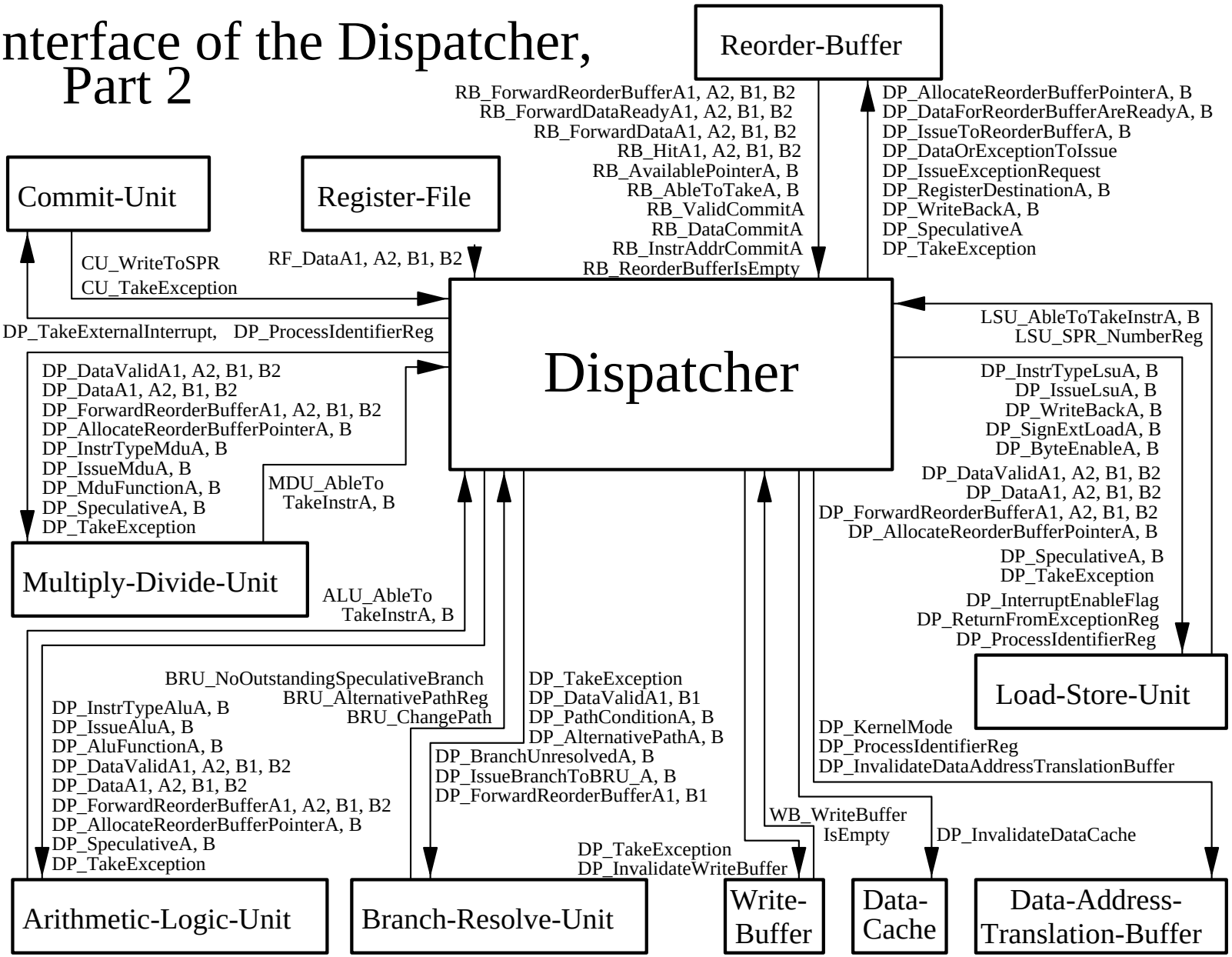
Interface of the Branch-Target-Buffer



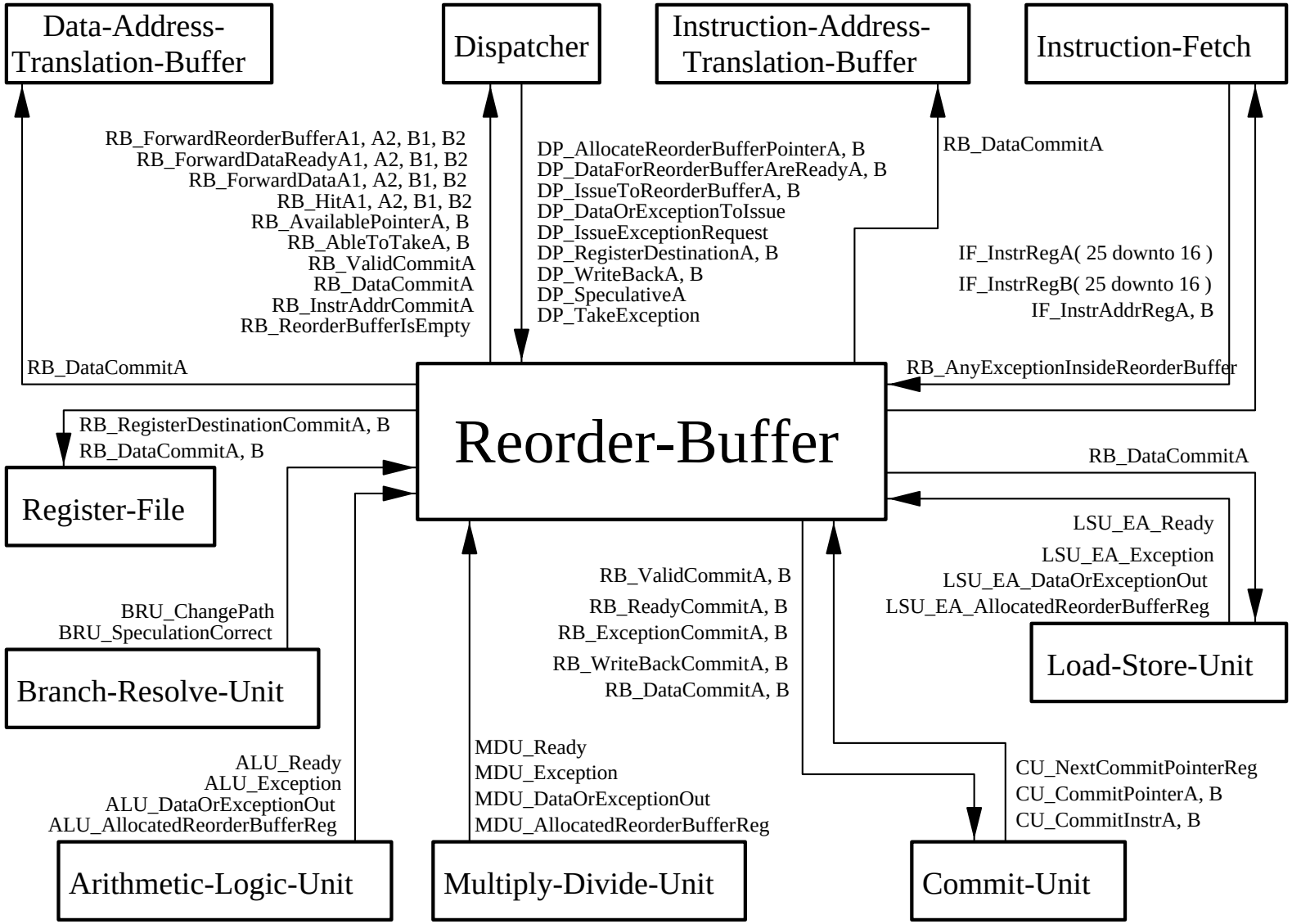
Interface of the Dispatcher, Part 1



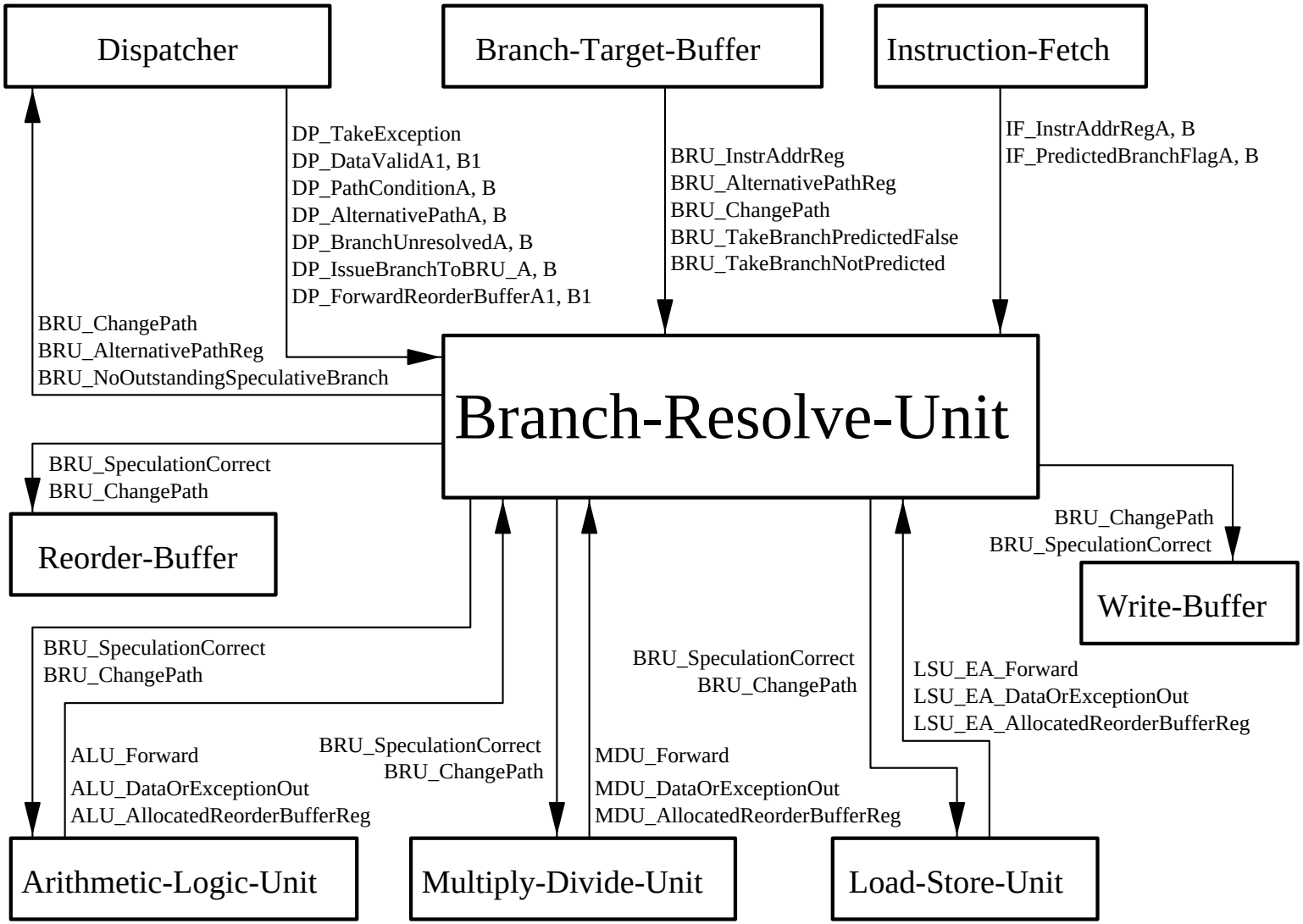
Interface of the Dispatcher, Part 2



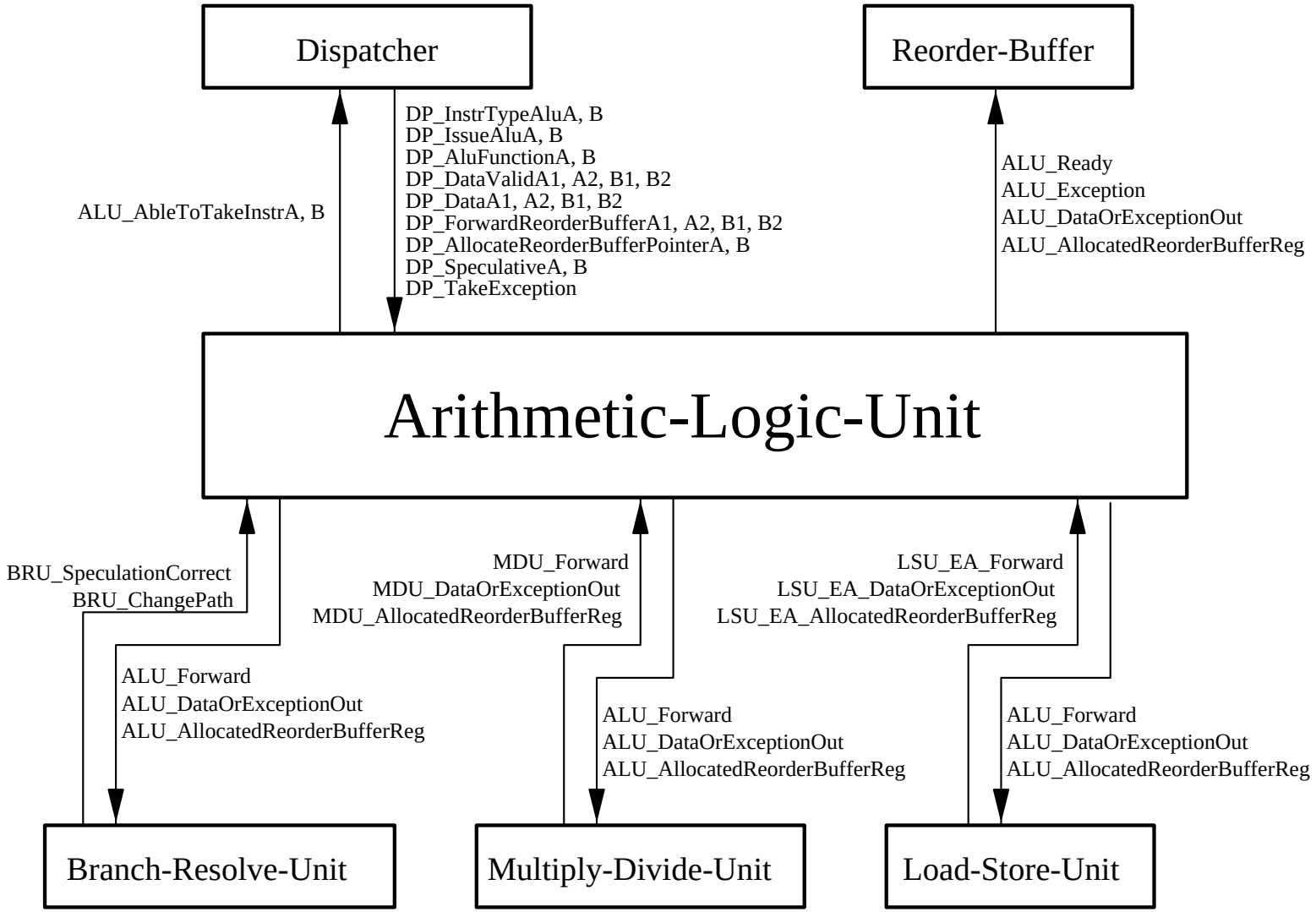
Interface of the Reorder-Buffer



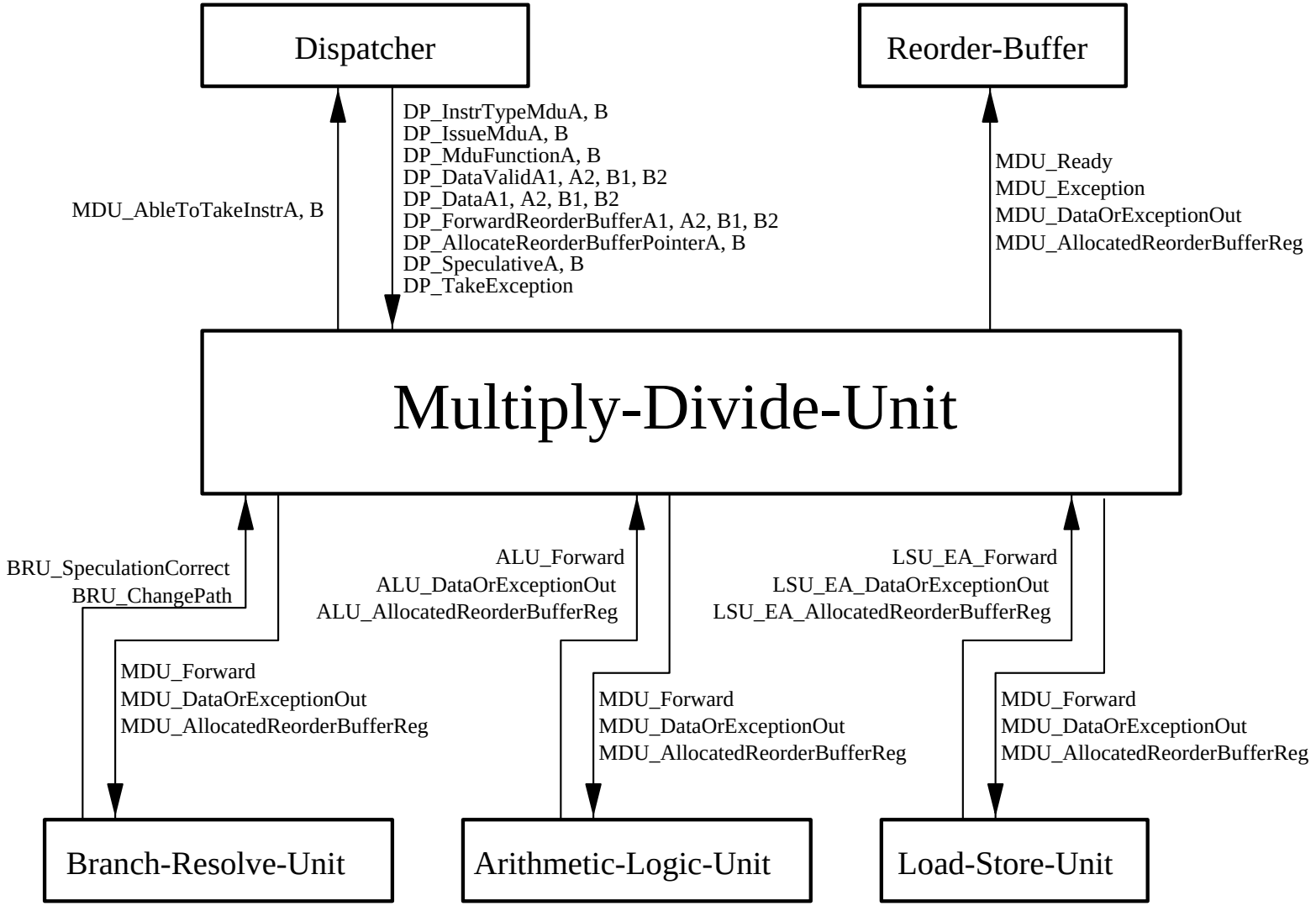
Interface of the Branch-Resolve-Unit



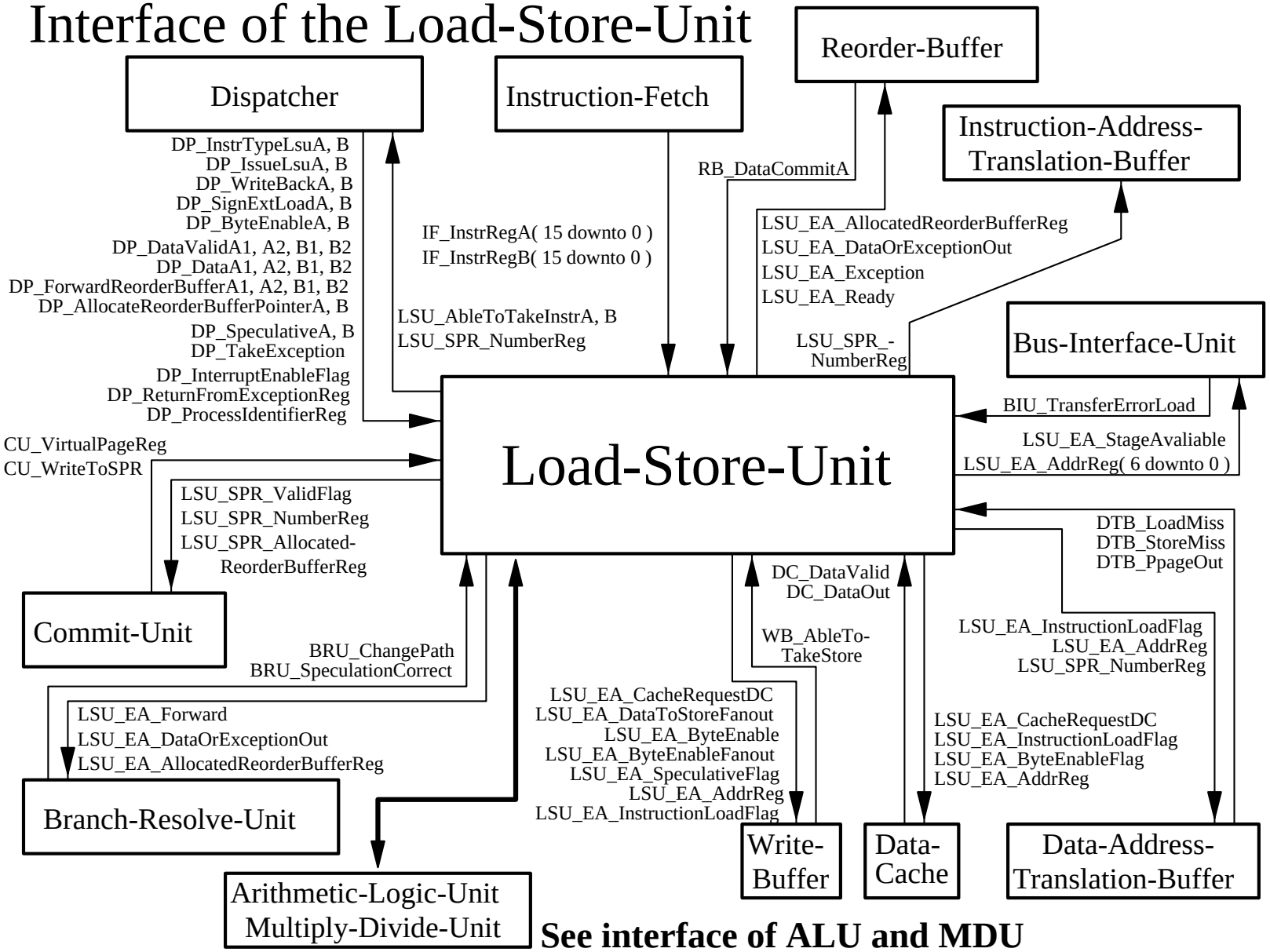
Interface of the Arithmetic-Logic-Unit



Interface of the Multiply-Divide-Unit

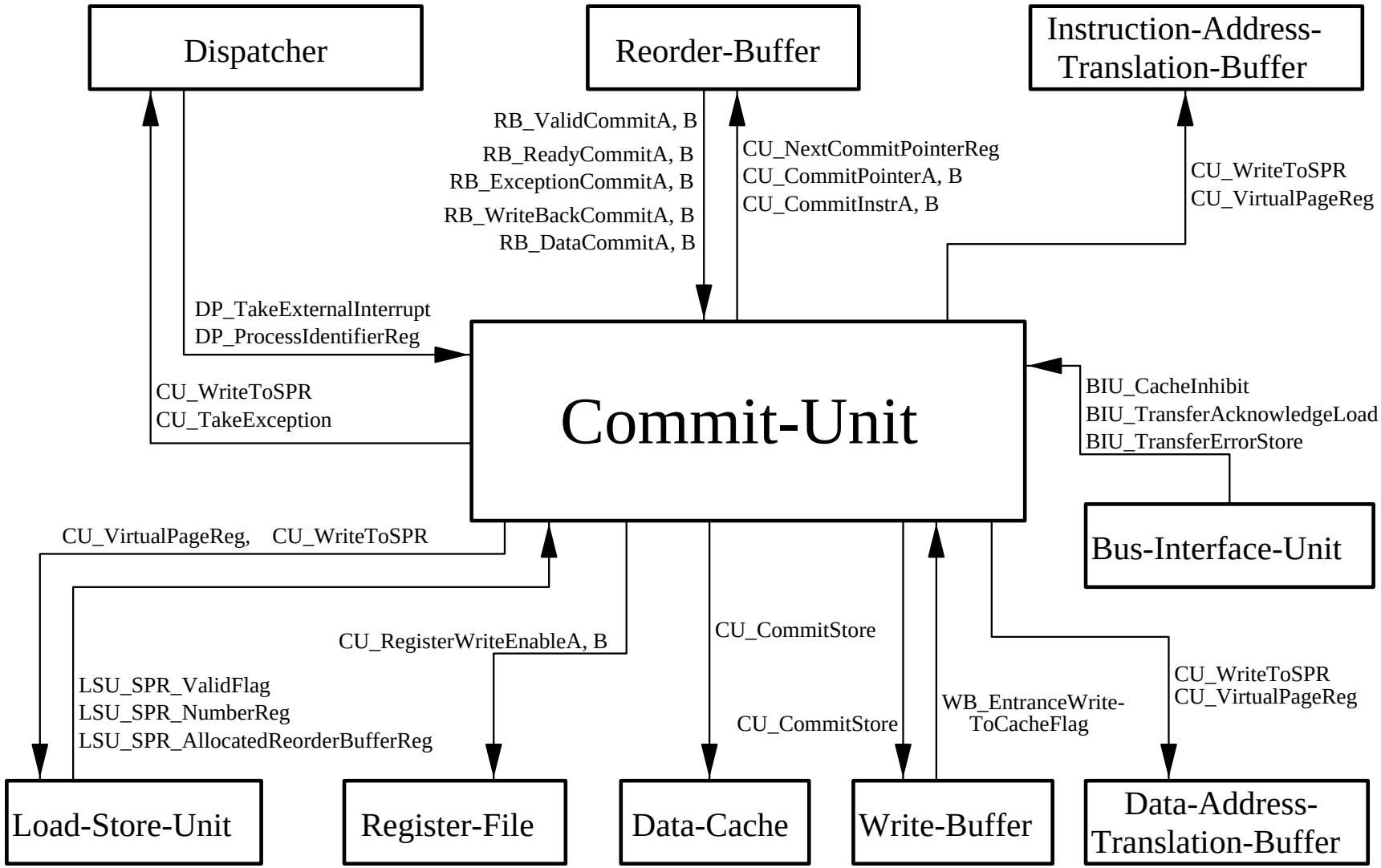


Interface of the Load-Store-Unit

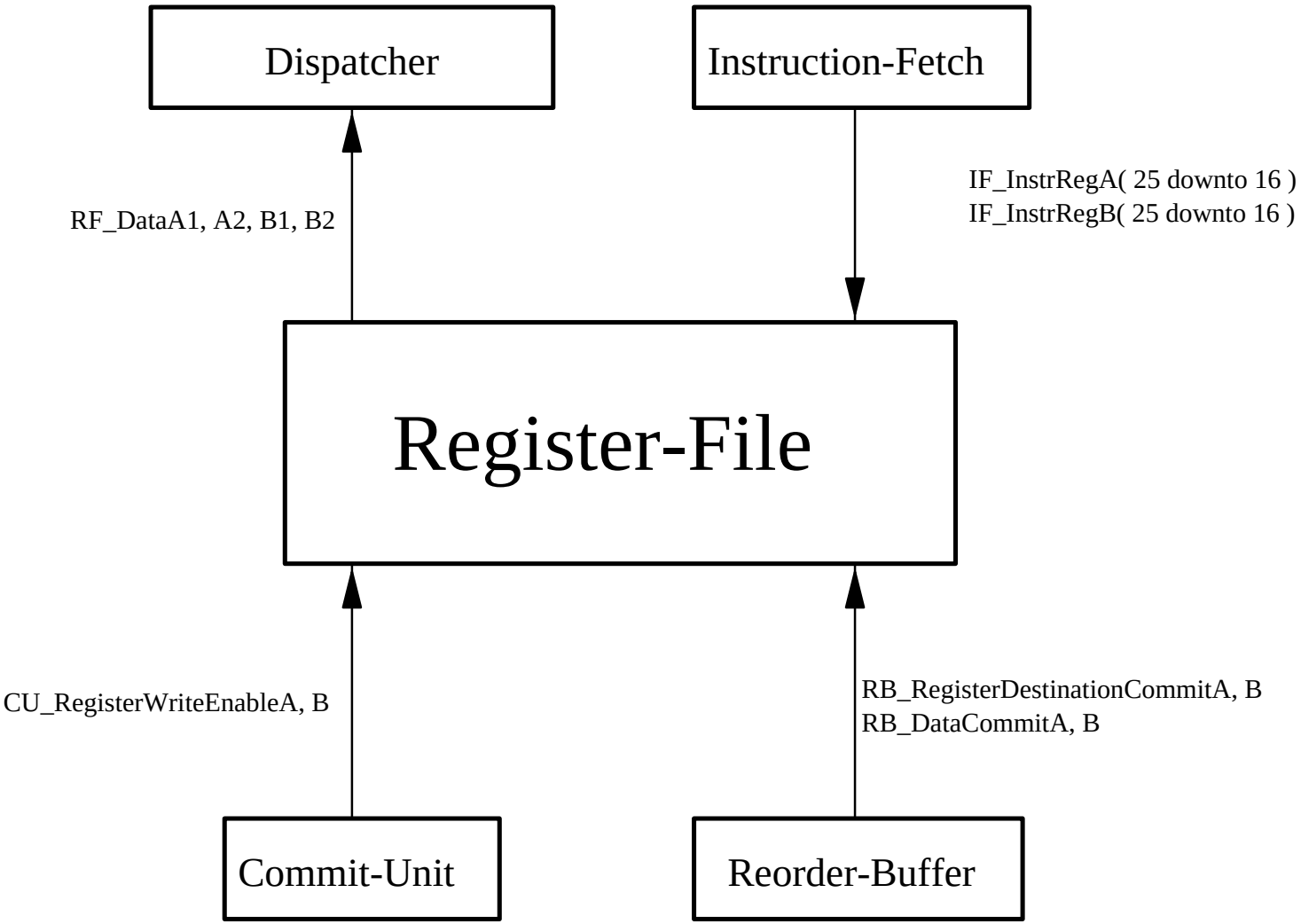


See interface of ALU and MDU

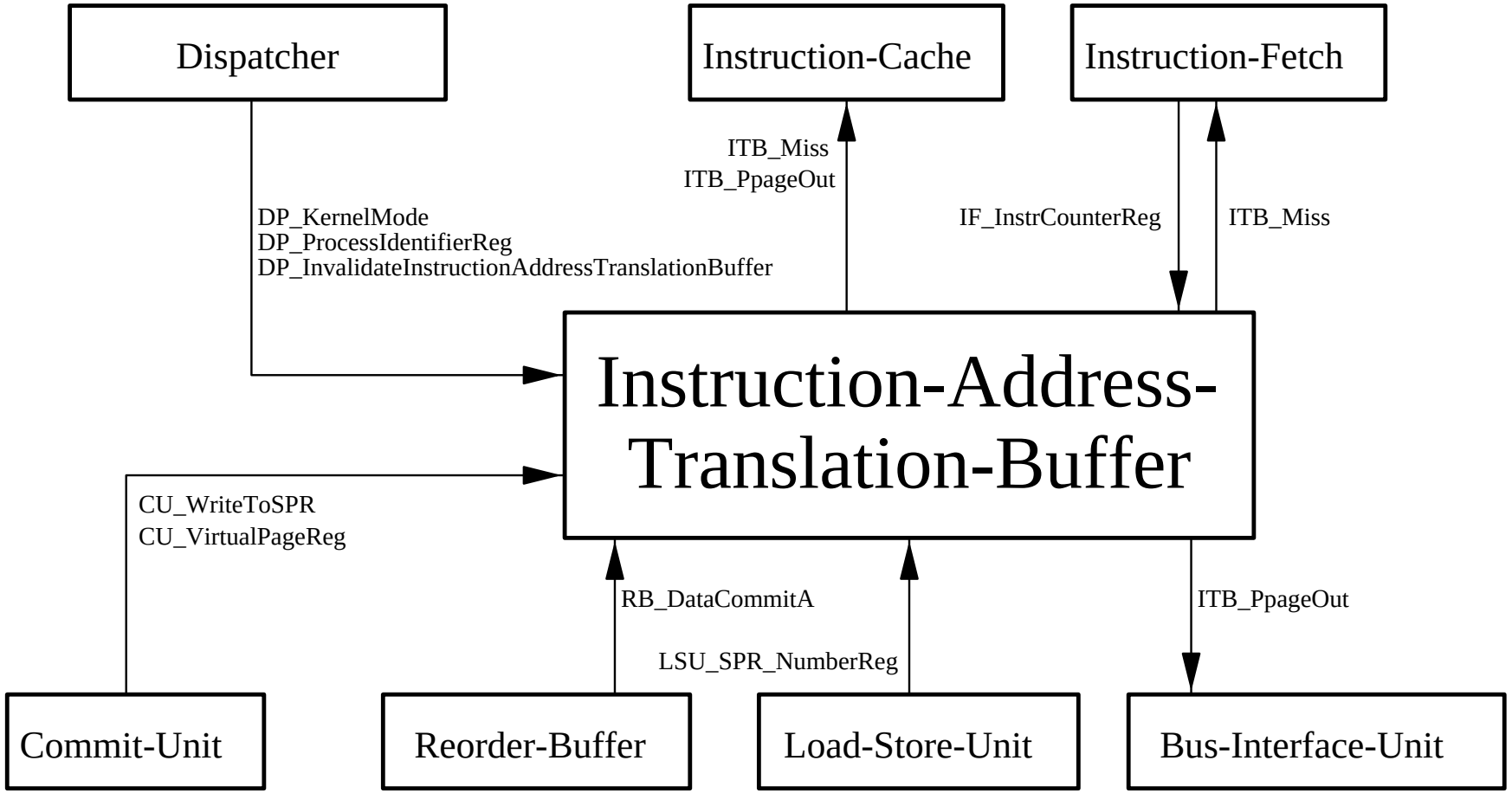
Interface of the Commit-Unit



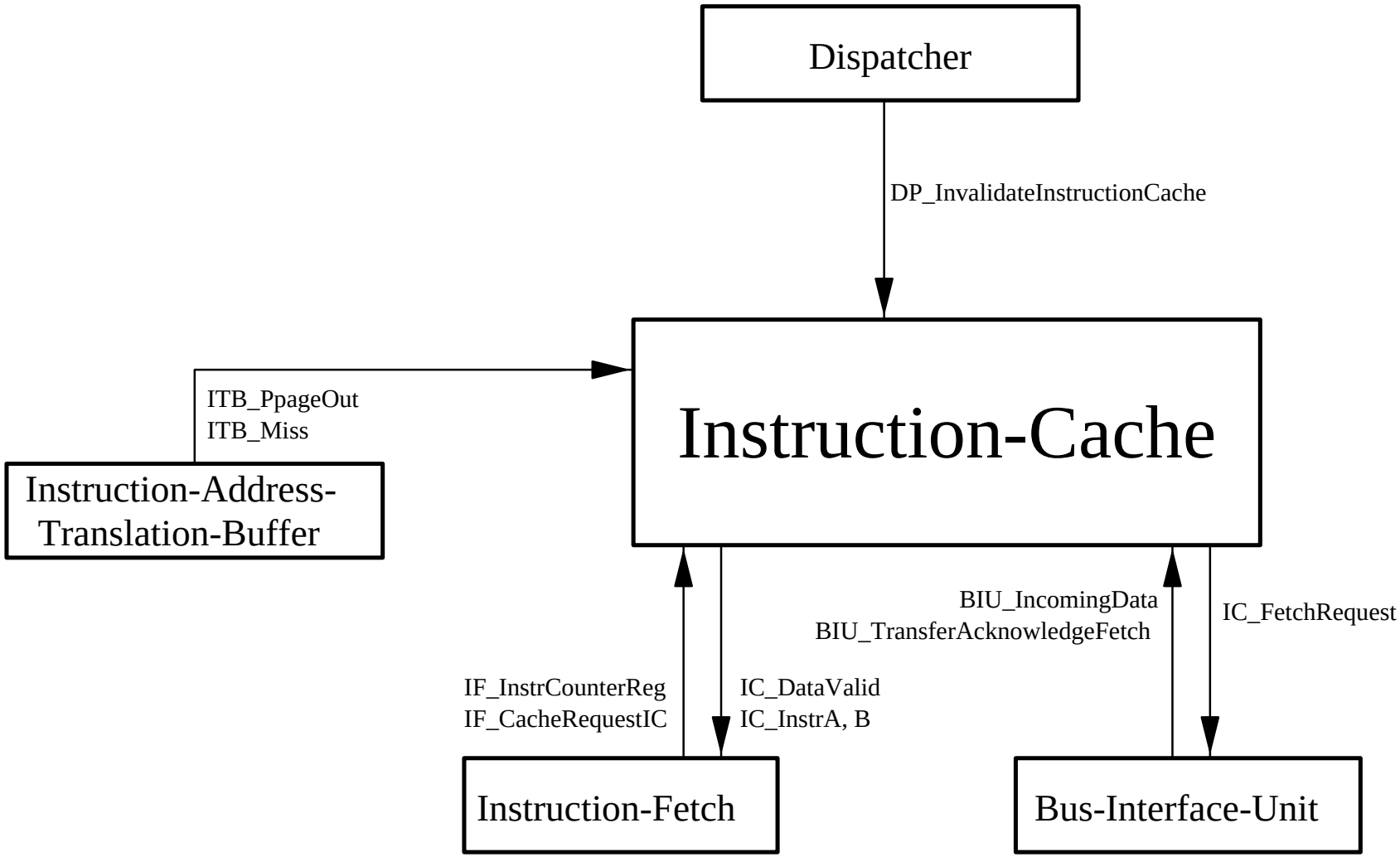
Interface of the Register-File



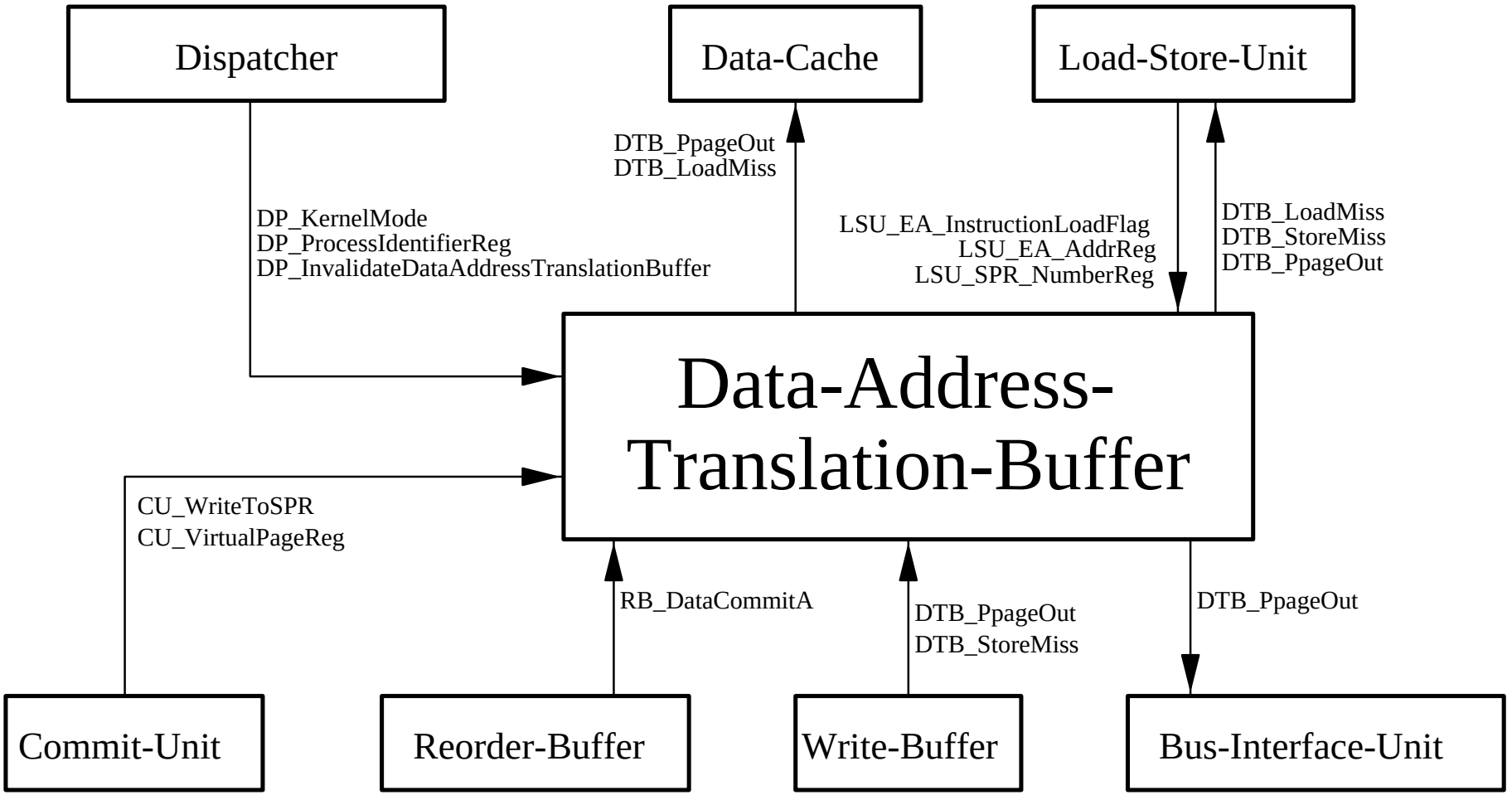
Interface of the Instruction-Address-Translation-Buffer



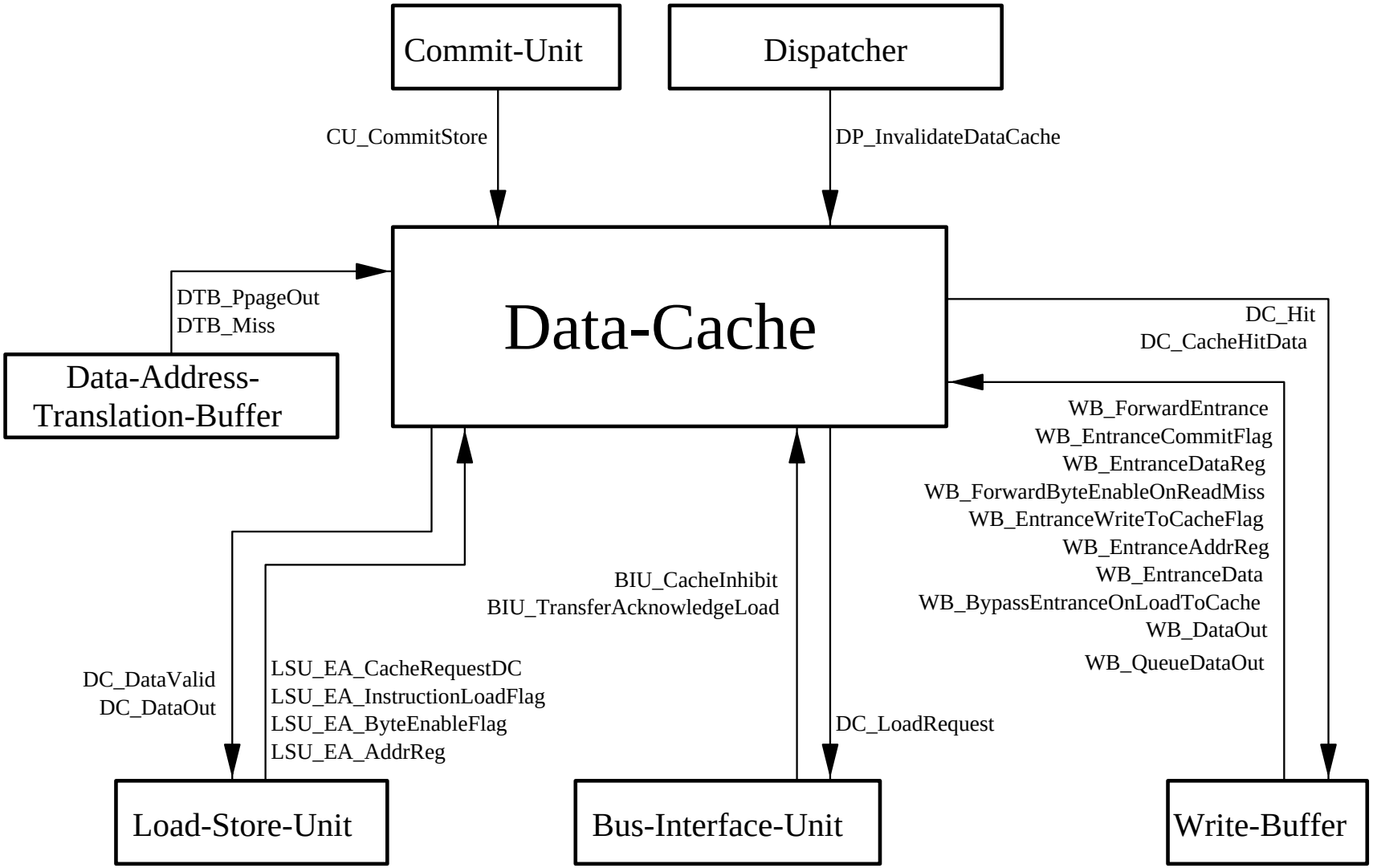
Interface of the Instruction-Cache



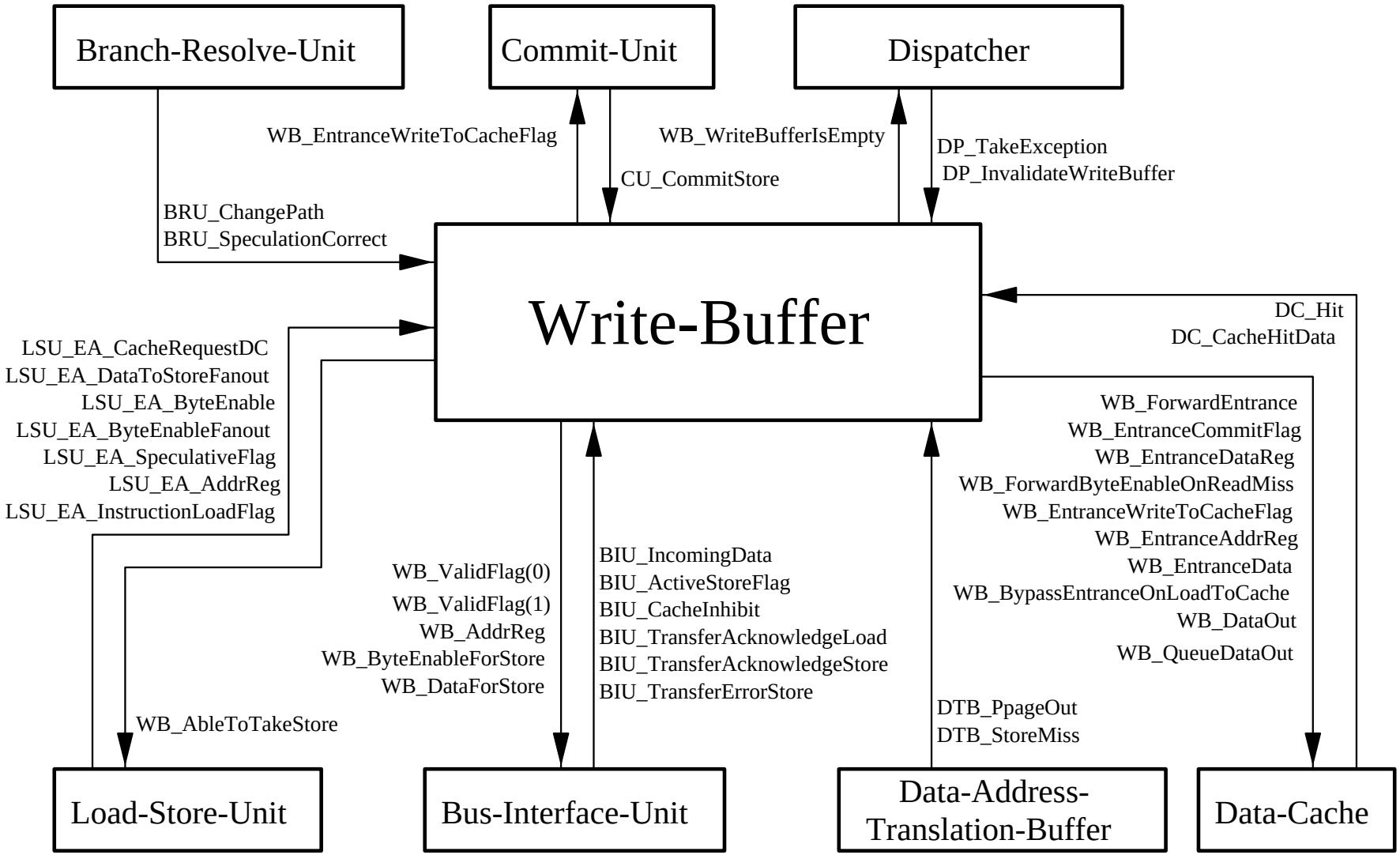
Interface of the Data-Address-Translation-Buffer



Interface of the Data-Cache



Interface of the Write-Buffer



Interface of the Bus-Interface-Unit