Tabellarische Darstellung des Befehlsflusses durch die Pipeline

Die folgenden Tabellen zeigen einige Registerinhalte aus der Simulation des Programms 'Demo.asm'. Diese werden durch Kommentare ergänzt. Die Tabellen sollen helfen, den Fluß der Befehle durch die Pipeline zu verfolgen.

Clock: 0, 1, 2, 3, 4, 5, 6

IF_InstrCounterReg	0000_0000	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	

Clock: 7

IF_InstrCounterReg	0000_0008	
IF_InstrRegA	jal Program (Addr: 0000_0000)	execute, new path, Reorder-Buffer: index 0
IF_InstrRegB	trap 0x104 (Addr: 0000_0004)	not in program flow

Clock: 8

IF_InstrCounterReg	0000_2000	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(0)	valid	jal Program
RB_ReadyFlag(0)	ready	jal Program

Clock: 9, 10, 11, 12

IF_InstrCounterReg	0000_2000	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(0)	invalid	
RF_Reg(31)	0000_0004	
Comment	Pipe is empty	

Clock: 13

IF_InstrCounterReg	0000_2008	
IF_InstrRegA	addui r1,r0,List + 4 (Addr: 0000_2000)	issue, Reorder-Buffer: index 1
IF_InstrRegB	addui r2,r0,1 (Addr: 0000_2004)	resource not available, wait

Clock: 14

IF_InstrCounterReg	0000_2008	
IF_InstrRegA	addui r2,r0,1 (Addr: 0000_2004)	issue, Reorder-Buffer: index 2
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	addui r1,r0,List + 4
RB_ReadyFlag(1)	not ready	addui r1,r0,List + 4

Clock: 15

IF_InstrCounterReg	0000_2008	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	addui r1,r0,List + 4
RB_ReadyFlag(1)	ready	addui r1,r0,List + 4
RB_ValidFlag(2)	valid	addui r2,r0,1
RB_ReadyFlag(2)	not ready	addui r2,r0,1

Clock: 16

IF_InstrCounterReg	0000_2008	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	invalid	
RB_ValidFlag(2)	valid	addui r2,r0,1
RB_ReadyFlag(2)	ready	addui r2,r0,1
RF_Reg(1)	0000_3004	

Clock: 17

IF_InstrCounterReg	0000_2008	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(2)	invalid	
RF_Reg(2)	0000_0001	
Comment	Pipe is empty	

Clock: 19

IF_InstrCounterReg	0000_2010	
IF_InstrRegA	sw -0x80(r0),r2 (Addr: 0000_2008)	issue, Reorder-Buffer: index 3
IF_InstrRegB	add r3,r0,r2 (Addr: 0000_200C)	issue, Reorder-Buffer: index 4

Clock: 20

IF_InstrCounterReg	0000_2010	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(3)	valid	sw -0x80(r0),r2
RB_ReadyFlag(3)	not ready	sw -0x80(r0),r2
RB_ValidFlag(4)	valid	add r3,r0,r2
RB_ReadyFlag(4)	not ready	add r3,r0,r2

Clock: 21

IF_InstrCounterReg	0000_2010	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(3)	valid	sw -0x80(r0),r2
RB_ReadyFlag(3)	not ready	sw -0x80(r0),r2
RB_ValidFlag(4)	valid	add r3,r0,r2
RB_ReadyFlag(4)	ready	add r3,r0,r2

Clock: 22

IF_InstrCounterReg	0000_2010	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(3)	valid	sw -0x80(r0),r2
RB_ReadyFlag(3)	ready	sw -0x80(r0),r2
RB_ValidFlag(4)	valid	add r3,r0,r2
RB_ReadyFlag(4)	ready	add r3,r0,r2

Clock: 23, 24

IF_InstrCounterReg	0000_2010	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(3)	invalid	
RB_ValidFlag(4)	invalid	
DP_InterruptEnableFlag	enabled	
RF_Reg(3)	0000_0001	
Comment	Pipe is empty	

Clock: 25

IF_InstrCounterReg	0000_2018	
IF_InstrRegA	lhu r4,CountLoops(r0) (Addr: 0000_2010)	issue, Reorder-Buffer: index 0
IF_InstrRegB	sw -4(r1),r2 (Addr: 0000_2014)	resource not available, wait

Clock: 26

IF_InstrCounterReg	0000_2018	
IF_InstrRegA	sw -4(r1),r2 (Addr: 0000_2014)	issue, Reorder-Buffer: index 1
IF_InstrRegB	invalid	
RB_ValidFlag(0)	valid	lhu r4,CountLoops(r0)
RB_ReadyFlag(0)	not ready	lhu r4,CountLoops(r0)

Clock: 27, 28, 29, 30

IF_InstrCounterReg	0000_2018	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(0)	valid	lhu r4,CountLoops(r0)
RB_ReadyFlag(0)	not ready	lhu r4,CountLoops(r0)
RB_ValidFlag(1)	valid	sw -4(r1),r2
RB_ReadyFlag(1)	not ready	sw -4(r1),r2

Clock: 31, 32, 33

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	sw 0(r1),r3 (Addr: 0000_2018)	resource not available, wait
IF_InstrRegB	add r2,r2,r3 (Addr: 0000_201C)	blocked by previous instruction, wait
Comment	Instructions in Reorder-Buffer can not proceed	waiting for load

Clock: 34

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	sw 0(r1),r3 (Addr: 0000_2018)	issue, Reorder-Buffer: index 2
IF_InstrRegB	add r2,r2,r3 (Addr: 0000_201C)	issue, Reorder-Buffer: index 3
RB_ValidFlag(0)	valid	lhu r4,CountLoops(r0)
RB_ReadyFlag(0)	not ready	lhu r4,CountLoops(r0)
RB_ValidFlag(1)	valid	sw -4(r1),r2
RB_ReadyFlag(1)	not ready	sw -4(r1),r2

Clock: 35

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(0)	valid	lhu r4,CountLoops(r0)
RB_ReadyFlag(0)	ready	lhu r4,CountLoops(r0)
RB_ValidFlag(1)	valid	sw -4(r1),r2
RB_ReadyFlag(1)	not ready	sw -4(r1),r2
RB_ValidFlag(2)	valid	sw 0(r1),r3
RB_ReadyFlag(2)	not ready	sw 0(r1),r3
RB_ValidFlag(3)	valid	add r2,r2,r3
RB_ReadyFlag(3)	not ready	add r2,r2,r3

Clock: 36

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(0)	invalid	
RB_ValidFlag(1)	valid	sw -4(r1),r2
RB_ReadyFlag(1)	ready	sw -4(r1),r2
RB_ValidFlag(2)	valid	sw 0(r1),r3
RB_ReadyFlag(2)	not ready	sw 0(r1),r3
RB_ValidFlag(3)	valid	add r2,r2,r3
RB_ReadyFlag(3)	ready	add r2,r2,r3
RF_Reg(4)	0000_0003	

Clock: 37

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	invalid	
RB_ValidFlag(2)	valid	sw 0(r1),r3
RB_ReadyFlag(2)	ready	sw 0(r1),r3
RB_ValidFlag(3)	valid	add r2,r2,r3
RB_ReadyFlag(3)	ready	add r2,r2,r3

Clock: 38

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(2)	invalid	
RB_ValidFlag(3)	invalid	
RF_Reg(2)	0000_0002	
Comment	Pipe is empty	

Clock: 39

IF_InstrCounterReg	0000_2028	
IF_InstrRegA	sw 4(r1),r2 (Addr: 0000_2020)	issue, Reorder-Buffer: index 4
IF_InstrRegB	addui r1,r1,8 (Addr: 0000_2024)	issue, Reorder-Buffer: index 0

Clock: 40

IF_InstrCounterReg	0000_2028	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(4)	valid	sw 4(r1),r2
RB_ReadyFlag(4)	not ready	sw 4(r1),r2
RB_ValidFlag(0)	valid	addui r1,r1,8
RB_ReadyFlag(0)	not ready	addui r1,r1,8

Clock: 41

IF_InstrCounterReg	0000_2028	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(4)	valid	sw 4(r1),r2
RB_ReadyFlag(4)	not ready	sw 4(r1),r2
RB_ValidFlag(0)	valid	addui r1,r1,8
RB_ReadyFlag(0)	ready	addui r1,r1,8

Clock: 42

IF_InstrCounterReg	0000_2028	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(4)	valid	sw 4(r1),r2
RB_ReadyFlag(4)	ready	sw 4(r1),r2
RB_ValidFlag(0)	valid	addui r1,r1,8
RB_ReadyFlag(0)	ready	addui r1,r1,8

Clock: 43, 44, 45, 46

IF_InstrCounterReg	0000_2028	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(4)	invalid	
RB_ValidFlag(0)	invalid	
RF_Reg(1)	0000_300C	
Comment	Pipe is empty	

Clock: 47

IF_InstrCounterReg	0000_2030	
IF_InstrRegA	add r3,r2,r3 (Addr: 0000_2028)	issue, Reorder-Buffer: index 1
IF_InstrRegB	sub r4,r4,1 (Addr: 0000_202C)	resource not available, wait

Clock: 48

IF_InstrCounterReg	0000_2030	
IF_InstrRegA	sub r4,r4,1 (Addr: 0000_202C)	issue, Reorder-Buffer: index 2
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	add r3,r2,r3
RB_ReadyFlag(1)	not ready	add r3,r2,r3

Clock: 49

IF_InstrCounterReg	0000_2030	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	add r3,r2,r3
RB_ReadyFlag(1)	ready	add r3,r2,r3
RB_ValidFlag(2)	valid	sub r4,r4,1
RB_ReadyFlag(2)	not ready	sub r4,r4,1

Clock: 50

IF_InstrCounterReg	0000_2030	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	invalid	
RB_ValidFlag(2)	valid	sub r4,r4,1
RB_ReadyFlag(2)	ready	sub r4,r4,1
RF_Reg(3)	0000_0003	

Clock: 51, 52, 53, 54

IF_InstrCounterReg	0000_2030	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	invalid	
RB_ValidFlag(2)	invalid	
RF_Reg(4)	0000_0002	
Comment	Pipe is empty	

Clock: 55

IF_InstrCounterReg	0000_2038	
IF_InstrRegA	bnez r4,Loop (Addr: 0000_2030)	execute, new path
IF_InstrRegB	addui r7,r0,List (Addr: 0000_2034)	not in program flow
Comment	Pipe is empty	

Clock: 56

IF_InstrCounterReg	0000_2018	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	

Clock: 57

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	sw 0(r1),r3 (Addr: 0000_2018)	issue, Reorder-Buffer: index 3
IF_InstrRegB	add r2,r2,r3 (Addr: 0000_201C)	issue, Reorder-Buffer: index 4

Clock: 58

IF_InstrCounterReg	0000_2028	
IF_InstrRegA	sw 4(r1),r2 (Addr: 0000_2020)	issue, Reorder-Buffer: index 0
IF_InstrRegB	addui r1,r1,8 (Addr: 0000_2024)	issue, Reorder-Buffer: index 1
RB_ValidFlag(3)	valid	sw 0(r1),r3
RB_ReadyFlag(3)	not ready	sw 0(r1),r3
RB_ValidFlag(4)	valid	add r2,r2,r3
RB_ReadyFlag(4)	not ready	add r2,r2,r3

Clock: 59

IF_InstrCounterReg	0000_2030	
IF_InstrRegA	add r3,r2,r3 (Addr: 0000_2028)	issue, Reorder-Buffer: index 2
IF_InstrRegB	sub r4,r4,1 (Addr: 0000_202C)	resource not available, wait
RB_ValidFlag(3)	valid	sw 0(r1),r3
RB_ReadyFlag(3)	not ready	sw 0(r1),r3
RB_ValidFlag(4)	valid	add r2,r2,r3
RB_ReadyFlag(4)	ready	add r2,r2,r3
RB_ValidFlag(0)	valid	sw 4(r1),r2
RB_ReadyFlag(0)	not ready	sw 4(r1),r2
RB_ValidFlag(1)	valid	addui r1,r1,8
RB_ReadyFlag(1)	not ready	addui r1,r1,8
Comment	Hit in Branch-Target-Buffer (0000_2030)	

Clock: 60

IF_InstrCounterReg	0000_2018	branch was predicted
IF_InstrRegA	sub r4,r4,1 (Addr: 0000_202C)	issue, Reorder-Buffer: index 3
IF_InstrRegB	bnez r4,Loop (Addr: 0000_2030)	unresolved, issue to Branch-Resolve-Unit
RB_ValidFlag(3)	valid	sw 0(r1),r3
RB_ReadyFlag(3)	ready	sw 0(r1),r3
RB_ValidFlag(4)	valid	add r2,r2,r3
RB_ReadyFlag(4)	ready	add r2,r2,r3
RB_ValidFlag(0)	valid	sw 4(r1),r2
RB_ReadyFlag(0)	not ready	sw 4(r1),r2
RB_ValidFlag(1)	valid	addui r1,r1,8
RB_ReadyFlag(1)	ready	addui r1,r1,8
RB_ValidFlag(2)	valid	add r3,r2,r3
RB_ReadyFlag(2)	not ready	add r3,r2,r3
Comment	Reorder-Buffer if full	

Clock: 61

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	sw 0(r1),r3 (Addr: 0000_2018)	issue speculative, Reorder-Buffer: index 4
IF_InstrRegB	add r2,r2,r3 (Addr: 0000_201C)	issue speculative, Reorder-Buffer: index 0
RB_ValidFlag(0)	valid	sw 4(r1),r2
RB_ReadyFlag(0)	ready	sw 4(r1),r2
RB_ValidFlag(1)	valid	addui r1,r1,8
RB_ReadyFlag(1)	ready	addui r1,r1,8
RB_ValidFlag(2)	valid	add r3,r2,r3
RB_ReadyFlag(2)	ready	add r3,r2,r3
RB_ValidFlag(3)	valid	sub r4,r4,1
RB_ReadyFlag(3)	not ready	sub r4,r4,1
RB_ValidFlag(4)	invalid	
RF_Reg(2)	0000_0005	
Comment	Unresolved branch in Branch-Resolve-Unit	The Commit-Unit is not able to commit all ready instructions

Clock: 62

IF_InstrCounterReg	0000_2028	
IF_InstrRegA	sw 4(r1),r2 (Addr: 0000_2020)	issue, Reorder-Buffer: index 1
IF_InstrRegB	addui r1,r1,8 (Addr: 0000_2024)	issue, Reorder-Buffer: index 2
RB_ValidFlag(2)	valid	add r3,r2,r3
RB_ReadyFlag(2)	ready	add r3,r2,r3
RB_ValidFlag(3)	valid	sub r4,r4,1
RB_ReadyFlag(3)	ready	sub r4,r4,1
RB_ValidFlag(4)	valid	sw 0(r1),r3
RB_SpeculativeFlag(4)	speculative	sw 0(r1),r3
RB_ReadyFlag(4)	not ready	sw 0(r1),r3
RB_ValidFlag(0)	valid	add r2,r2,r3
RB_SpeculativeFlag(0)	speculative	add r2,r2,r3
RB_ReadyFlag(0)	not ready	add r2,r2,r3
RB_ValidFlag(1)	invalid	
RF_Reg(1)	0000_3014	
Comment	Branch in Branch-Resolve-Unit resolved as correct	

Clock: 63

IF_InstrCounterReg	0000_2030	
IF_InstrRegA	add r3,r2,r3 (Addr: 0000_2028)	issue, Reorder-Buffer: index 3
IF_InstrRegB	sub r4,r4,1 (Addr: 0000_202C)	resource not available, wait
RB_ValidFlag(4)	valid	sw 0(r1),r3
RB_SpeculativeFlag(4)	not speculative	sw 0(r1),r3
RB_ReadyFlag(4)	not ready	sw 0(r1),r3
RB_ValidFlag(0)	valid	add r2,r2,r3
RB_SpeculativeFlag(0)	not speculative	add r2,r2,r3
RB_ReadyFlag(0)	ready	add r2,r2,r3
RB_ValidFlag(1)	valid	sw 4(r1),r2
RB_ReadyFlag(1)	not ready	sw 4(r1),r2
RB_ValidFlag(2)	valid	addui r1,r1,8
RB_ReadyFlag(2)	not ready	addui r1,r1,8
RB_ValidFlag(3)	invalid	
RF_Reg(3)	0000_0008	
RF_Reg(4)	0000_0001	
Comment	Hit in Branch-Target-Buffer (0000_2030)	

Clock: 64

IF_InstrCounterReg	0000_2018	branch was predicted
IF_InstrRegA	sub r4,r4,1 (Addr: 0000_202C)	issue, Reorder-Buffer: index 4
IF_InstrRegB	bnez r4,Loop (Addr: 0000_2030)	unresolved, issue to Branch-Resolve-Unit
RB_ValidFlag(4)	valid	sw 0(r1),r3
RB_ReadyFlag(4)	ready	sw 0(r1),r3
RB_ValidFlag(0)	valid	add r2,r2,r3
RB_ReadyFlag(0)	ready	add r2,r2,r3
RB_ValidFlag(1)	valid	sw 4(r1),r2
RB_ReadyFlag(1)	not ready	sw 4(r1),r2
RB_ValidFlag(2)	valid	addui r1,r1,8
RB_ReadyFlag(2)	ready	addui r1,r1,8
RB_ValidFlag(3)	valid	add r3,r2,r3
RB_ReadyFlag(3)	not ready	add r3,r2,r3
Comment	Reorder-Buffer if full	

Clock: 65

IF_InstrCounterReg	0000_2020	
IF_InstrRegA	sw 0(r1),r3 (Addr: 0000_2018)	issue speculative, Reorder-Buffer: index 0
IF_InstrRegB	add r2,r2,r3 (Addr: 0000_201C)	issue speculative, Reorder-Buffer: index 1
RB_ValidFlag(1)	valid	sw 4(r1),r2
RB_ReadyFlag(1)	ready	sw 4(r1),r2
RB_ValidFlag(2)	valid	addui r1,r1,8
RB_ReadyFlag(2)	ready	addui r1,r1,8
RB_ValidFlag(3)	valid	add r3,r2,r3
RB_ReadyFlag(3)	ready	add r3,r2,r3
RB_ValidFlag(4)	valid	sub r4,r4,1
RB_ReadyFlag(4)	not ready	sub r4,r4,1
RB_ValidFlag(0)	invalid	
RF_Reg(2)	0000_000D	
Comment	Unresolved branch in Branch-Resolve-Unit	The Commit-Unit is not able to commit all ready instructions

Clock: 66

IF_InstrCounterReg	0000_2028	
IF_InstrRegA	sw 4(r1),r2 (Addr: 0000_2020)	wrong speculation, invalidate stage
IF_InstrRegB	addui r1,r1,8 (Addr: 0000_2024)	wrong speculation, invalidate stage
RB_ValidFlag(3)	valid	add r3,r2,r3
RB_ReadyFlag(3)	ready	add r3,r2,r3
RB_ValidFlag(4)	valid	sub r4,r4,1
RB_ReadyFlag(4)	ready	sub r4,r4,1
RB_ValidFlag(0)	valid	sw 0(r1),r3
RB_SpeculativeFlag(0)	speculative	sw 0(r1),r3
RB_ReadyFlag(0)	not ready	sw 0(r1),r3
RB_ValidFlag(1)	valid	add r2,r2,r3
RB_SpeculativeFlag(1)	speculative	add r2,r2,r3
RB_ReadyFlag(1)	not ready	add r2,r2,r3
RB_ValidFlag(2)	invalid	
RF_Reg(1)	0000_301C	
Comment	The speculative instruction will be canceled because speculation was wrong	

Clock: 67

IF_InstrCounterReg	0000_2034	alternative path from Branch-Resolve-Unit
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(3)	invalid	
RB_ValidFlag(4)	invalid	
RB_ValidFlag(0)	invalid	
RB_ValidFlag(1)	invalid	
RF_Reg(3)	0000_0015	
RF_Reg(4)	0000_0000	
Comment	Pipe is empty	

Clock: 68

IF_InstrCounterReg	0000_2038	
IF_InstrRegA	addui r7,r0,List (Addr: 0000_2034)	issue, Reorder-Buffer: index 0
IF_InstrRegB	invalid	

Clock: 69

IF_InstrCounterReg	0000_2038	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(0)	valid	addui r7,r0,List
RB_ReadyFlag(0)	not ready	addui r7,r0,List

Clock: 70

IF_InstrCounterReg	0000_2038	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(0)	valid	addui r7,r0,List
RB_ReadyFlag(0)	ready	addui r7,r0,List

Clock: 71, 72, 73, 74

IF_InstrCounterReg	0000_2038	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(0)	invalid	
RF_Reg(7)	0000_3000	
Comment	Pipe is empty	

Clock: 75, 76, 77, 78

IF_InstrCounterReg	0000_2040	
IF_InstrRegA	trap 0x104 (Addr: 0000_2038)	wait until Write-Buffer is empty
IF_InstrRegB	sw -0x100(r0),r7 (Addr: 0000_203C)	

Clock: 79

IF_InstrCounterReg	0000_2040	
IF_InstrRegA	trap 0x104 (Addr: 0000_2038)	wait until Write-Buffer is empty, done
IF_InstrRegB	sw -0x100(r0),r7 (Addr: 0000_203C)	issue, Reorder-Buffer: index 1

Clock: 80

IF_InstrCounterReg	0000_2040	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	sw -0x100(r0),r7
RB_ReadyFlag(1)	not ready	sw -0x100(r0),r7

Clock: 81

IF_InstrCounterReg	0000_2040	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	sw -0x100(r0),r7
RB_ReadyFlag(1)	not ready	sw -0x100(r0),r7
Comment	Take external interrupt	

Clock: 82

IF_InstrCounterReg	0000_0A00	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	invalid	
DP_ReturnFromExceptionReg	0000_203D	
DP_InterruptEnableFlag	disabled	

Clock: 83, 84, 85, 86

IF_InstrCounterReg	0000_0A00	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	

Clock: 87

IF_InstrCounterReg	0000_0A08	
IF_InstrRegA	lw r30,-0xc0(r0) (Addr: 0000_0A00)	issue, Reorder-Buffer: index 1
IF_InstrRegB	nop (Addr: 0000_0A04)	stage A only

Clock: 88

IF_InstrCounterReg	0000_0A08	
IF_InstrRegA	nop (Addr: 0000_0A04)	done
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	lw r30,-0xc0(r0)
RB_ReadyFlag(1)	not ready	lw r30,-0xc0(r0)

Clock: 89, 90, 91, 92

IF_InstrCounterReg	0000_0A08	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	lw r30,-0xc0(r0)
RB_ReadyFlag(1)	not ready	lw r30,-0xc0(r0)

Clock: 93, 94, 95, 96

IF_InstrCounterReg	0000_0A10	
IF_InstrRegA	rfe (Addr: 0000_0A08)	wait until Reorder-Buffer is empty
IF_InstrRegB	nop (Addr: 0000_0A0C)	
RB_ValidFlag(1)	valid	lw r30,-0xc0(r0)
RB_ReadyFlag(1)	not ready	lw r30,-0xc0(r0)

Clock: 97

IF_InstrCounterReg	0000_0A10	
IF_InstrRegA	rfe (Addr: 0000_0A08)	wait until Reorder-Buffer is empty
IF_InstrRegB	nop (Addr: 0000_0A0C)	
RB_ValidFlag(1)	valid	lw r30,-0xc0(r0)
RB_ReadyFlag(1)	ready	lw r30,-0xc0(r0)

Clock: 98

IF_InstrCounterReg	0000_0A10	
IF_InstrRegA	rfe (Addr: 0000_0A08)	execute, change path
IF_InstrRegB	nop (Addr: 0000_0A0C)	not in program flow
RB_ValidFlag(1)	invalid	
RF_Reg(30)	0000_0000	dummy
Comment	Pipe is empty, The RFE instruction enables a new external interrup request	take exception

Clock: 99

IF_InstrCounterReg	0000_0A00	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	

Clock: 100

IF_InstrCounterReg	0000_0A08	
IF_InstrRegA	lw r30,-0xc0(r0) (Addr: 0000_0A00)	issue, Reorder-Buffer: index 2
IF_InstrRegB	nop (Addr: 0000_0A04)	stage A only

Clock: 101

IF_InstrCounterReg	0000_0A0C	
IF_InstrRegA	nop (Addr: 0000_0A04)	done
IF_InstrRegB	rfe (Addr: 0000_0A08)	stage A only
RB_ValidFlag(2)	valid	lw r30,-0xc0(r0)
RB_ReadyFlag(2)	not ready	lw r30,-0xc0(r0)

Clock: 102, 103, 104, 105, 106

IF_InstrCounterReg	0000_0A10	
IF_InstrRegA	rfe (Addr: 0000_0A08)	wait until Reorder-Buffer is empty
IF_InstrRegB	nop (Addr: 0000_0A0C)	
RB_ValidFlag(1)	valid	lw r30,-0xc0(r0)
RB_ReadyFlag(1)	not ready	lw r30,-0xc0(r0)
Comment	There is no Data-Cache hit because the load was cache inhibited	

Clock: 107

IF_InstrCounterReg	0000_0A10	
IF_InstrRegA	rfe (Addr: 0000_0A08)	wait until Reorder-Buffer is empty
IF_InstrRegB	nop (Addr: 0000_0A0C)	
RB_ValidFlag(1)	valid	lw r30,-0xc0(r0)
RB_ReadyFlag(1)	ready	lw r30,-0xc0(r0)

Clock: 108

IF_InstrCounterReg	0000_0A10	
IF_InstrRegA	rfe (Addr: 0000_0A08)	execute, change path
IF_InstrRegB	nop (Addr: 0000_0A0C)	not in program flow
RB_ValidFlag(1)	invalid	
RF_Reg(30)	0000_0000	dummy
Comment	Pipe is empty	

Clock: 109

IF_InstrCounterReg	0000_203C	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
DP_InterruptEnableFlag	enabled	

Clock: 110

IF_InstrCounterReg	0000_2040	
IF_InstrRegA	sw -0x100(r0),r7 (Addr: 0000_203C)	issue, Reorder-Buffer: index 3
IF_InstrRegB	invalid	

Clock: 111, 112

IF_InstrCounterReg	0000_2040	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(3)	valid	sw -0x100(r0),r7
RB_ReadyFlag(3)	not ready	sw -0x100(r0),r7

Clock: 113

IF_InstrCounterReg	0000_2040	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(3)	valid	sw -0x100(r0),r7
RB_ReadyFlag(3)	ready	sw -0x100(r0),r7

Clock: 114

IF_InstrCounterReg	0000_2040	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(3)	invalid	
Comment	Pipe is empty	

Clock: 115

IF_InstrCounterReg	0000_2048	
IF_InstrRegA	addui r7,r0,20 (Addr: 0000_2040)	issue, Reorder-Buffer: index 4
IF_InstrRegB	trap 0x104 (Addr: 0000_2044)	stage A only

Clock: 116

IF_InstrCounterReg	0000_2048	
IF_InstrRegA	trap 0x104 (Addr: 0000_2044)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	
RB_ValidFlag(4)	valid	addui r7,r0,20
RB_ReadyFlag(4)	not ready	addui r7,r0,20

Clock: 117

IF_InstrCounterReg	0000_2048	
IF_InstrRegA	trap 0x104 (Addr: 0000_2044)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	
RB_ValidFlag(4)	valid	addui r7,r0,20
RB_ReadyFlag(4)	ready	addui r7,r0,20

Clock: 118

IF_InstrCounterReg	0000_2048	
IF_InstrRegA	trap 0x104 (Addr: 0000_2044)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	
RB_ValidFlag(4)	invalid	
RF_Reg(7)	0000_0014	
Comment	Pipe is empty	

Clock: 119, 120

IF_InstrCounterReg	0000_2048	
IF_InstrRegA	trap 0x104 (Addr: 0000_2044)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	

Clock: 121, 122, 123, 124

IF_InstrCounterReg	0000_204C	
IF_InstrRegA	trap 0x104 (Addr: 0000_2044)	wait until Write-Buffer is empty
IF_InstrRegB	sw -0xfc(r0),r7 (Addr: 0000_2048)	

Clock: 125

IF_InstrCounterReg	0000_204C	
IF_InstrRegA	trap 0x104 (Addr: 0000_2044)	wait until Write-Buffer is empty, done
IF_InstrRegB	sw -0xfc(r0),r7 (Addr: 0000_2048)	issue, Reorder-Buffer: index 0

Clock: 126, 127

IF_InstrCounterReg	0000_2050	
IF_InstrRegA	trap 0x104 (Addr: 0000_204C)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	
RB_ValidFlag(0)	valid	sw -0xfc(r0),r7
RB_ReadyFlag(0)	not ready	sw -0xfc(r0),r7

Clock: 128

IF_InstrCounterReg	0000_2050	
IF_InstrRegA	trap 0x104 (Addr: 0000_204C)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	
RB_ValidFlag(0)	valid	sw -0xfc(r0),r7
RB_ReadyFlag(0)	ready	sw -0xfc(r0),r7

Clock: 129, 130

IF_InstrCounterReg	0000_2050	
IF_InstrRegA	trap 0x104 (Addr: 0000_204C)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	
RB_ValidFlag(0)	invalid	
Comment	Pipe is empty	

Clock: 131, 132, 133, 134

IF_InstrCounterReg	0000_2054	
IF_InstrRegA	trap 0x104 (Addr: 0000_204C)	wait until Write-Buffer is empty
IF_InstrRegB	sw -0xf8(r0),r0 (Addr: 0000_2050)	

Clock: 135

IF_InstrCounterReg	0000_2054	
IF_InstrRegA	trap 0x104 (Addr: 0000_204C)	wait until Write-Buffer is empty, done
IF_InstrRegB	sw -0xf8(r0),r0 (Addr: 0000_2050)	issue, Reorder-Buffer: index 1

Clock: 136

IF_InstrCounterReg	0000_2058	
IF_InstrRegA	sw -0x1000(r0),r0 (Addr: 0000_2054)	issue, Reorder-Buffer: index 2
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	sw -0xf8(r0),r0
RB_ReadyFlag(1)	not ready	sw -0xf8(r0),r0

Clock: 137

IF_InstrCounterReg	0000_2058	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	sw -0xf8(r0),r0
RB_ReadyFlag(1)	not ready	sw -0xf8(r0),r0
RB_ValidFlag(2)	valid	sw -0x1000(r0),r0
RB_ReadyFlag(2)	not ready	sw -0x1000(r0),r0

Clock: 138

IF_InstrCounterReg	0000_2058	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	valid	sw -0xf8(r0),r0
RB_ReadyFlag(1)	ready	sw -0xf8(r0),r0
RB_ValidFlag(2)	valid	sw -0x1000(r0),r0
RB_ReadyFlag(2)	not ready	sw -0x1000(r0),r0

Clock: 139

IF_InstrCounterReg	0000_2058	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(1)	invalid	
RB_ValidFlag(2)	valid	sw -0x1000(r0),r0
RB_ReadyFlag(2)	ready	sw -0x1000(r0),r0

Clock: 140

IF_InstrCounterReg	0000_2058	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
RB_ValidFlag(2)	invalid	
Comment	Pipe is empty	

Clock: 141

IF_InstrCounterReg	0000_2060	
IF_InstrRegA	jr r31 (Addr: 0000_2058)	execute, change path
IF_InstrRegB	.word (Addr: 0000_205C)	not in program flow

Clock: 142, 143, 144, 145, 146, 147, 148

IF_InstrCounterReg	0000_0004	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	

Clock: 149, 150, 151

IF_InstrCounterReg	0000_0008	
IF_InstrRegA	trap 0x104 (Addr: 0000_0004)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	

Clock: 152

IF_InstrCounterReg	0000_0008	
IF_InstrRegA	trap 0x104 (Addr: 0000_0004)	wait until Write-Buffer is empty
IF_InstrRegB	invalid	
Comment	Transfer-Error for store, recognized on leading edge of Bus-Clock	take exception

Clock: 153

IF_InstrCounterReg	0000_0100	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
DP_ReturnFromExceptionReg	0000_0005	
DP_InterruptEnableFlag	disabled	

Clock: 154, 155, 156, 157, 158

IF_InstrCounterReg	0000_0100	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	

Clock: 159

IF_InstrCounterReg	0000_0108	
IF_InstrRegA	trap 0x104 (Addr: 0000_0100)	wait until Write-Buffer is empty, done
IF_InstrRegB	trap 0x0 (Addr: 0000_0104)	halt processor, stage A only

Clock: 160

IF_InstrCounterReg	0000_0108	
IF_InstrRegA	trap 0x0 (Addr: 0000_0104)	halt processor, execute
IF_InstrRegB	invalid	

Clock: 161

IF_InstrCounterReg	0000_0108	
IF_InstrRegA	invalid	
IF_InstrRegB	invalid	
DP_HaltFlag	processor halted	